Remarks/Arguments:

Claims 1, 2, 4, 6, 7, 9 - 12, 15 and 18 have been amended. Claim 17 has been cancelled. Claims 21-24 have been added. No new material is introduced herein. Claims 1-16 and 18-24 are pending.

Claim 11 has been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Namely, that the phrase "using the second set of timings to provide a forth stress" is not enabled. Claim 11 has been amended to clarify the number of first stresses provided. Support for the amendment may be found, for example, p. 7, lines 11-15. Accordingly, Applicants respectfully request that the rejection of claim 11 be withdrawn.

Claims 1-3, 5, 7-8 and 11-14 have been rejected under 35 U.S.C. §102(b) as being anticipated by Giles et al. (U.S. Pat. No. 6,085,334). It is respectfully submitted, however, that these claims are now patentable over the cited art for the reasons set forth below.

Claim 1, as amended, includes features neither disclosed nor suggested by the cited art, namely:

> ...applying a first test stress to selected cells of the plurality of memory cells with a built-in self test, the first test stress providing a stress level that is outside of a predetermined range...
>
> ...applying a second test stress to the selected cells and the repaired cells with the built-in self test, the second test stress being different from the first test stress... (Emphasis Added)

These features are disclosed, for example, p. 6, line 21-p. 7, line 5; p. 10, lines 8-11; and Fig. 1.

Giles et al. disclose a method, in Fig. 5, for characterizing an environmentally sensitive defect based on a change in the repair state of a memory device over the operating range of the memory device (Col. 2, lines 61-64). Giles et al. generate a first repair state signature at a first operating condition and a second repair state signature at a second operating condition. According to Giles et al., "a memory device is rejected if there is a change in the repair state of the memory array over the operating range of the device" under the condition that the first repair signature is different from the second repair signature (Col. 2, line 64- Col. 3, line 6). Giles et al. disclose that the environmental condition for testing may include a voltage level,

temperature and frequency of operation (Col. 8, lines 8-11). Giles et al. do not disclose or suggest Applicants' claimed features of "applying a first test stress to selected cells of the plurality of memory cells... the first test stress providing a stress level that is outside of a predetermined range" (emphasis added). These features are neither disclosed nor suggested by Giles et al. Giles et al. is silent on providing a test stress that is outside of an operational condition range. Thus, Giles et al. do not include all of the features of claim 1. Accordingly, allowance of claim 1 is respectfully requested.

Claims 2, 3 and 5 include all of the features of claim 1 from which they depend. Accordingly, claims 2, 3 and 5 are also patentable over the cited art.

Claim 7, as amended, includes features neither disclosed nor suggested by the cited art, namely:

> ...applying a first set of timings to selected cells of the plurality of memory cells using built-in self test controls, the first set of timings being outside of a predetermined timing range...
>
> ...applying a second set of timings different from the first set of timings to the selected cells and the repaired cells using the built-in self test controls... (Emphasis Added)

Amended claim 12 includes a similar recitation. These features are disclosed, for example, p. 7, lines 6-26; p. 8, line 30- p. 9, line 6; p. 10, lines 8-15; and Figure 1.

Giles et al. are discussed above. Giles et al. do not disclose or suggest Applicants' claimed features of "applying a first set of timings to selected cells... the first set of timings being outside of a predetermined timing range" or "applying a second set of timings different from the first set of timings to the selected cells and the repaired cells..." (emphasis added). These features are neither disclosed nor suggested by Giles et al. Although Giles et al. disclose a frequency of operation for testing, Giles et al. is silent on providing a set of timings or that a first set of timings are outside of an operational timing. Therefore, Giles et al. cannot disclose or suggest that a second set of timings are different from the first set of timings. Thus, Giles et al. do not include all of the features of claim 7. Accordingly, allowance of claim 7 is respectfully requested.

Claims 8 and 11 include all of the features of claim 7 from which they depend. Accordingly, claims 8 and 11 are also patentable over the cited art.

Amended claim 12, although not identical to claim 7, includes features similar to claim 7 which are not disclosed or suggested in the cited art, namely: "providing a first plurality of timings and a second plurality of timings to built-in self test controls, the first plurality of timings being different from the second plurality of timings, the first plurality of timings being outside of a predetermined timing range." Giles et al. is discussed above and do not include all of the features of claim 12. Accordingly, allowance of claim 12 is respectfully requested.

Claims 13 and 14 include all of the features of claim 12 from which they depend. Accordingly, claims 13 and 14 are also patentable over the cited art.

Claims 15-20 have been rejected under 35 U.S.C. §102(e) as being anticipated by Templeton et al. (U.S. Pat. No. 6,973,605). It is respectfully submitted, however, that these claims are now patentable over the cited art for the reasons set forth below.

Claim 15, as amended, includes features neither disclosed nor suggested by the cited art, namely:

...a first delay circuit comprising...

...a first timer for applying a plurality of timings to the memory cells, the plurality of timings including an operational timing mode within a predetermined timing range, a plurality of relaxed timing modes that exceeds the predetermined timing range and a plurality of tightened timing modes that is less than the predetermined timing range...

...a second timer for modifying at least one of the plurality of timings...

...a second delay circuit coupled to the first delay circuit for modifying at least one of the plurality of timings to provide a timing that exceeds the plurality of relaxed timing modes...

These features are disclosed, for example, p. 11, lines 5-12; p. 11, line 20-p. 12, line 7; and Figs. 2-5.

Templeton et al. disclose, in Figs. 3 and 4, providing a stress clock signal 304 to perform a high stress BISR on an ASIC memory during power up or global reset of the ASIC or an internal clock signal 302 during normal operation of the memory array (Col. 7, lines 52-63). As shown in Fig. 4, a memory clock generator 402 provides an internal clock signal 302 and stress clock signal 304 to multiplexer 408 (Col. 8, line 66-Col. 9, line 3). Templeton et al. do not disclose or suggest Applicants' claimed features of "...a first delay circuit comprising... a first timer for applying a plurality of timings... including... a plurality of relaxed timing modes that exceeds the predetermined timing range" or "a second delay circuit coupled to the first delay

circuit... to provide a timing that exceeds the plurality of relaxed timing modes" (emphasis added). These features are neither disclosed nor suggested by Templeton et al. Furthermore, Templeton et al. do not disclose or suggest that the device is used for testing during manufacture of the embedded memory. Thus, Templeton et al. do not include all of the features of claim 15. Accordingly, allowance of claim 15 is respectfully requested.

Claim 16-20 include all of the features of claim 15 from which they depend. Accordingly, claims 16-20 are also patentable over the cited art.

Claims 4, 6 and 9 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Giles et al. and further in view of Templeton et al. Claims 4 and 6, however, also include all of the features of claim 1 from which they depend; and claim 9 includes all of the features of claim 7 from which it depends. Templeton et al. do not make up for the features that are lacking in Giles et al. Accordingly, claims 4, 6 and 9 are also patentable over the cited art.

Claim 10 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Giles et al. Claim 10, however, also includes all of the features of claim 7 from which it depends. As discussed above, Giles et al. do not include all of the features of claim 7. Accordingly, claim 10 is also patentable over the cited art.

Claims 21-24 have been added. No new matter is introduced herein. Support for claims 21, 23 and 24 can be found, for example, p. 10, lines 23-29. Support for claim 22 can be found, for example, p. 7, lines 6-26; p. 8, line 30-p. 9, line 6; p. 10, line 8-11; and Fig. 1. Accordingly, claims 21-24 are patentable over the cited art.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

LEA/dmg

Dated: June 30, 2006

☒ P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

☐ P.O. Box 1596
Wilmington, DE 19899
(302) 778-2500

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